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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

3D GRAPHICS ACCELERATOR
POWER VR™ μPD62011

The μPD62011 is a 3D graphics accelerator LSI designed for personal computers of the PowerVR 3D graphics processor family.

The μPD62011 realizes high performance system by adding functions such as bi-linear texture and 66-MHz PCI bus support to the μPD62010 and incorporating a circuit that supports geometry operations performed in the CPU.

FEATURES

- Pin-compatible/software-compatible with the μPD62010
- Interface conforming with PCI bus 2.1 (supports 66 MHz)
- On-chip hidden surface removal (Z buffer unnecessary, per pixel, 32-bit depth precision)
- Automatic shadow generation by hardware
- Per-pixel fogging
- 66-MHz operation
- On-chip geometry processing support circuit
- Texture mapping
  - Perspective correct texture mapping
  - MIP mapping
  - Bi-linear texture
  - 16-/8- bit texture
  - Translucent texture
  - Texture memory: 1 to 4 Mbytes
- Shading
  - Smooth shading
  - Flat shading/Highlighting
- Output Image
  - RGB/BGR 565 Packed, RGB/BGR 555 Packed
  - RGB/BGR 888 Packed/Unpacked
  - Little/Big endian pixel format
  - Maximum 1024 × 1024 resolution
- Supported API
  - Dedicated API (PowerSGL™)
  - Microsoft's Direct3D™

ARCHITECTURE

The PowerVR system is a 3D graphics technology featuring an original architecture in order to resolve the intrinsic cost/performance problem of conventional 3D graphics systems. The most typical functions, hidden surface removal and plane modeling, are described below.

1. Hidden Surface Removal

Conventional 3D graphics systems employ the Z-buffer that compares the z value (depth) of each polygon-configuring pixel when performing hidden surface removal (removing data invisible from the viewpoint). The memory requirement for 32-bit depth at 640 × 480 pixels is 1.2 Mbytes, which greatly affects the cost of the system. Moreover, because memory access must be executed the same number of times as the number of polygons that include the pixel for which hidden surface removal is to be performed, the system performance is affected by the memory band width (data transfer performance).

In the PowerVR architecture, the display is divided into 32 × 32 pixels or 64 × 64 pixels segments called tiles and hidden surface removal is performed within the device. Accordingly, since no Z-buffer is necessary and the data written into the frame buffer is only the forefront visible pixel data, high performance 3D systems not limited by the memory system can be realized.

2. Plane Modeling

In addition to the conventional polygon modeling method (configuring with triangles and squares), PowerVR employs the method of modeling with an infinite plane (defining an area enclosed by planes as an object). The data (x, y, z) of each vertex of the polyhedron that configures the object is required in the polygon modeling method. On the other hand, in plane modeling, data is defined using only a normal vector and a point on a plane, which considerably reduces the amount of data. This data reduction directly contributes to reducing the processing time. Additionally, a unique function that performs real-time and automatic shadow generation for effective 3D rendition by using plane modeling is realized.

OUTLINE OF μPD62011 FUNCTIONS

The μPD62011 extends the functions of the μPD62010 and improves 3D graphics rendering, while realizing high performance.

1. Bi-linear Texture Mapping

The μPD62010 employs the MIP mapping function for precise texture mapping. MIP mapping is a precise texture mapping method (2-point texture) in which the texture to be mapped is prepared in advance, and then data is sampled from a large and small texture sheets corresponding to the object.

The μPD62011 enhances the function of the μPD62010 and supports bi-linear texture mapping. In data sampling in the core of MIP mapping, mapping is performed by interpolating two points from each texture (4-point texture).

2. 66-MHz PCI Bus Interface

In the PowerVR system, the parameters/data for 3D image processing are captured via the PCI bus, and the generated 3D images are transferred to the 2D system via the PCI bus. The μPD62011 provides an interface compatible with the 66-MHz spec of PCI bus, which enables high-speed parameter transfer/image data transfer.

3. Floating Point Format Conversion Circuit

In the PowerVR system, parameters A and B of the plane equation Ax + By + C are processed in the 20-bit floating point format, and parameter C is processed in the 20-bit fixed point format.

In the μPD62010, conversion from the IEEE floating point format to the above data format is performed by software. On the other hand, the μPD62011, which incorporates a format conversion circuit, enables loading of parameter data in the IEEE floating point format which enables high-speed processing by reducing the software load.

4. On-chip Pointer Register

When loading the parameters or object data in the main memory, the μPD62010 references the pointer table configured in memory but the μPD62011 accesses data directly because it has a pointer register. Moreover, successive data loading is enabled by the pointer chain function.

5. Output Image Mask Function

Since the PowerVR architecture adopts 3D screen processing in tile units, when adding 3D objects on a 2D background, the background color of tiles must be made transparent. The μPD62010 does this by software, while, the μPD62011 does this by masking the output image in pixel units.

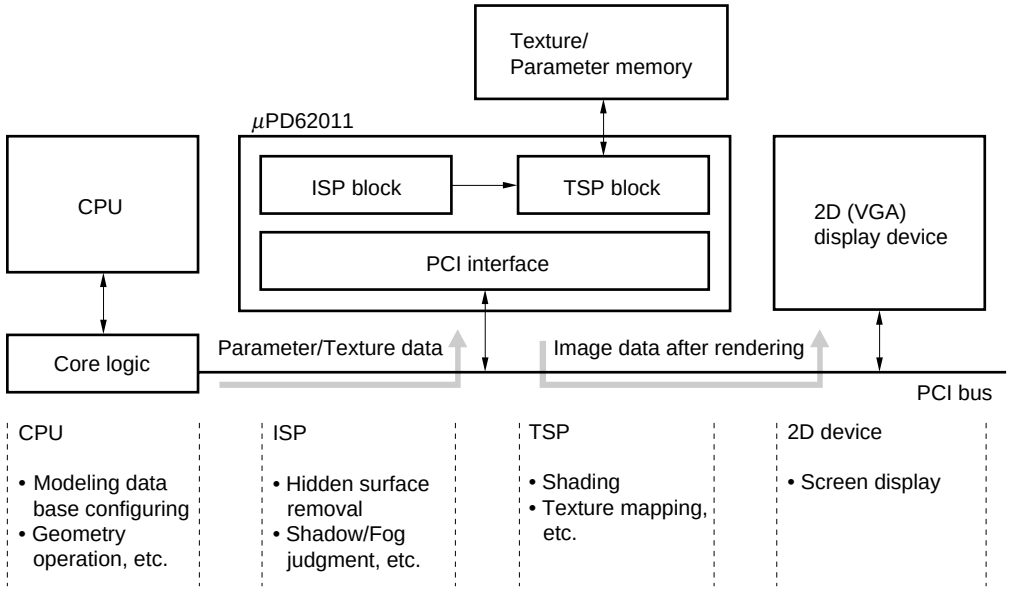
6. Edge Sharing

When processing a polygon mesh structure, the amount of data processing is reduced greatly by sharing the data regarding the boundary edges of neighboring polygons.

7. Software-Compatible with μPD62010

The μPD62011 is compatible with the μPD62010 in the initial state immediately after reset. This function is enabled by register setting.

INTERNAL BLOCK DIAGRAM



The main function of the ISP block is performing hidden surface removal for an object list in a 3D space. The output of the ISP block is the ID of the visible surface corresponding to each pixel. Hidden surface removal carried in the ISP block has a precision equivalent to that of conventional Z buffering. As a result, when processing with a precision identical that of a 32-bit Z buffer is performed, the μPD62011 does not require a Z buffer memory. Moreover, the ISP block supports the shadow casting function indicating whether a shadow is generated in the visible surface.

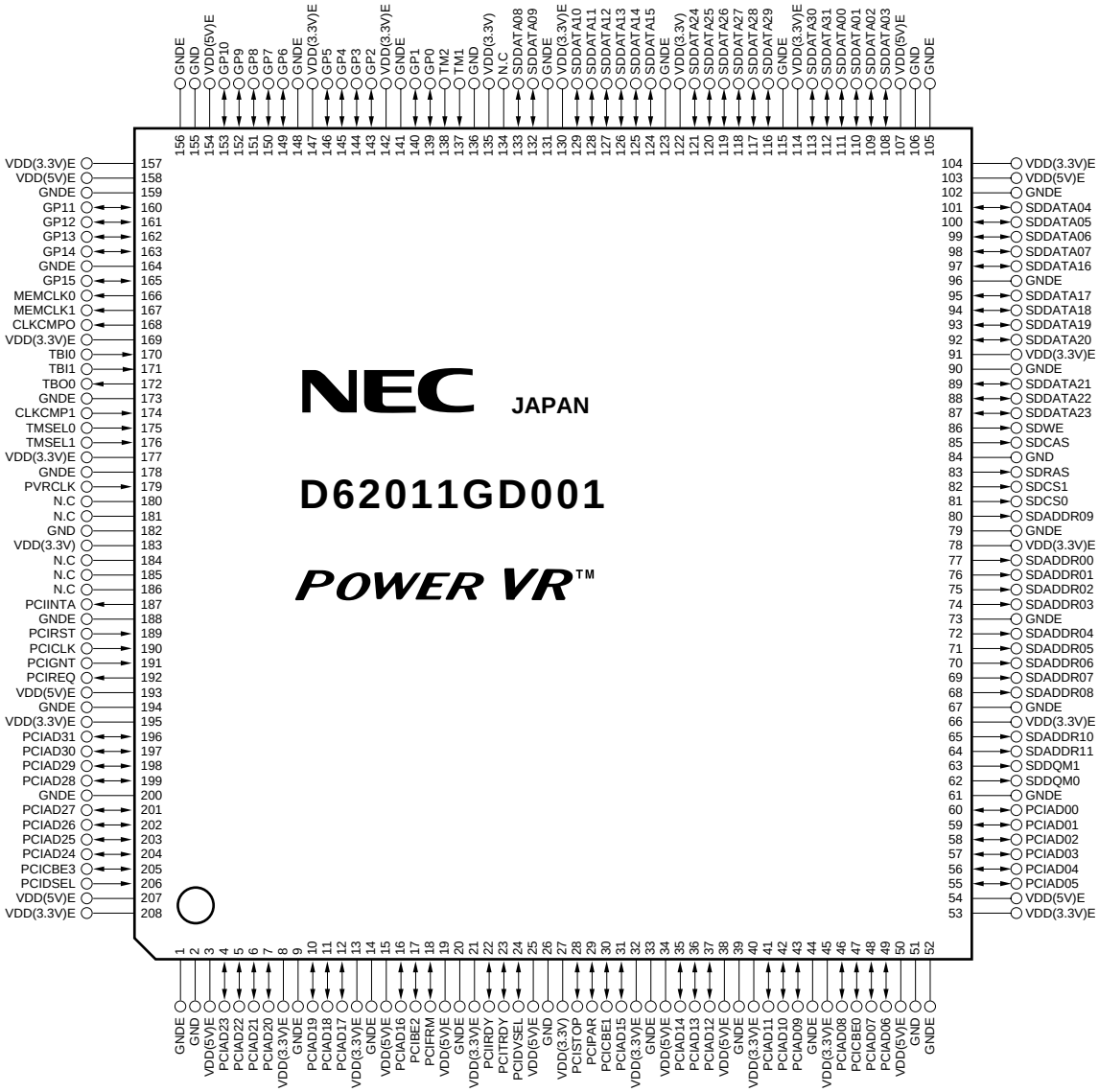
The TSP block mainly performs precise texture mapping and shading for the ID of the visible surface supplied by the ISP. The TSP also enables perspective correct texture mapping, smooth shading, transparent face overlaying, and fogging. Besides, the TSP block provides a method for processing visible surface with a minimum number of accesses to texture data stored in an external SDRAM. Both the ISP and TSP blocks have internal caches enabling an efficient local access for rendering parameters stored in these caches.

The PCI bus interface is provided with both master and slave functions for efficient operation. When the μPD62011 reads the parameters related to the ISP block from the system memory, the PCI bus interface functions as PCI master and when it receives the parameters related to the TSP block, it functions as a PCI slave. The PCI bus interface performs optimum buffering for transferring data securely at high speed. The SDRAM/SGRAM controller is designed to allow the blocks in the μPD62011 to share external SDRAM/SGRAM.

The μPD62011 receives the parameters required for rendering via PCI bus and transfers 3D images with texture mapping or shading to the PCI address space. The 3D images data from the μPD62011 is transferred to the 2D graphics (VGA™ controller) frame buffer allocated in the PCI address space.

PIN CONFIGURATION (Top View)

208-PIN PLASTIC QFP (28 × 28 mm)

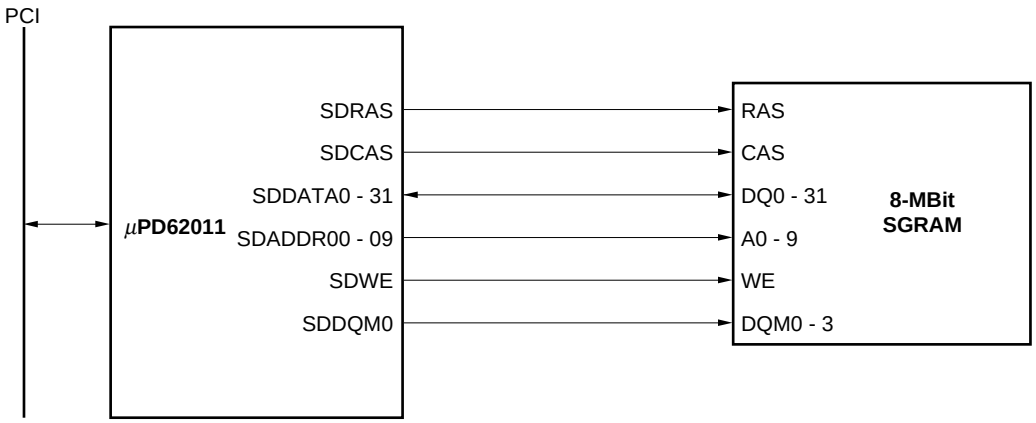


PIN FUNCTION LIST

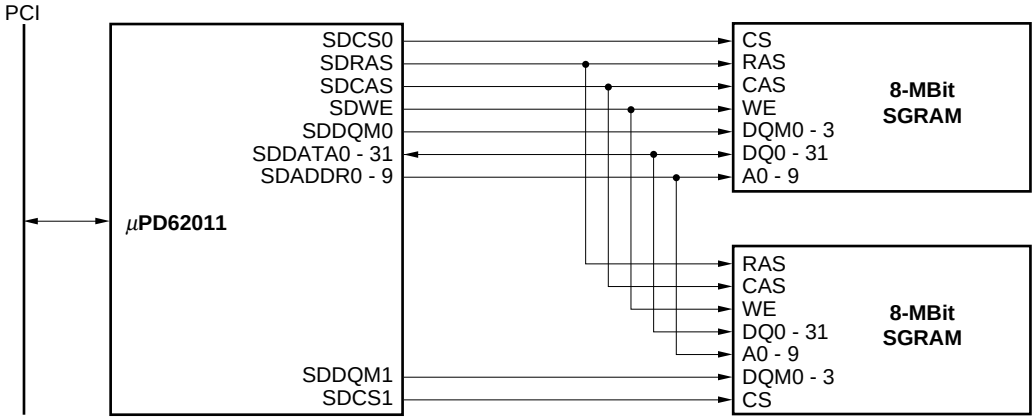
Pin Name	Function
PCIFRM	PCI Cycle Frame
PCIIRDY	PCI Initiator Ready
PCITRDY	PCI Target Ready
PCIDVSEL	PCI Device Select
PCISTOP	PCI Stop/Disconnect
PCIPAR	PCI Parity
PCIINTA	PCI Interrupt A
PCIRST	PCI Reset, used as master reset for the μPD62011
PCICLK	Clock for PCI Interface
PCIGNT	PCI Master Grant
PCIREQ	PCI Master Request
PCICBE0 to 3	PCI Bus Command and Byte Enables
PCIIDSEL	PCI Initialization Device Select
PCIAD00 to 31	PCI Address Data Bus
SDDQM0 to 1	Memory Request
SDADR00 to 11	Memory Address Bus
SDCS0 to 1	Memory Chip Select
SDRAS	Memory Row Address Strobe
SDCAS	Memory Column Address Strobe
SDWE	Memory Write Enable
SDDATA00 to 31	Memory Data Bus
GP0 to 15	General Purpose I/O Port
MEMCLK0 to 1	Memory Clock
CLKCMPO	Clock Adjusting Port (Output)
CLKCMPI	Clock Adjusting Port (Input)
PVRCLK	Internal Clock
TM1 to 2	Test Input
TBI0 to 1	Test Input
TBO0	Test Output
TMSEL0 to 1	Test Input
VDD (3.3 V)	Internal Digital VDD (3.3 V)
GND	Internal Digital GND
VDD (5 V) E	External Digital VDD (5 V)
VDD (3.3 V) E	External Digital VDD (3.3 V)
GNDE	External Digital GND

INTERFACE BETWEEN μPD62011 AND MEMORY

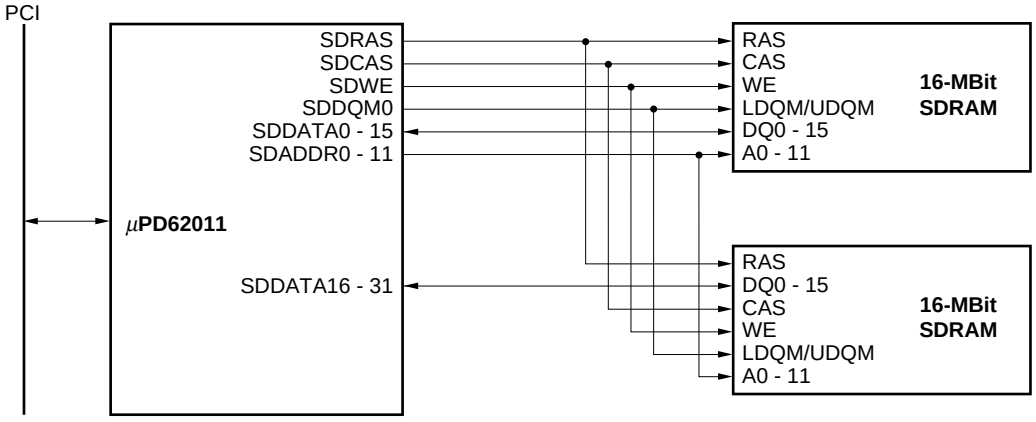
(1) 1 Mbyte



(2) 2 Mbytes



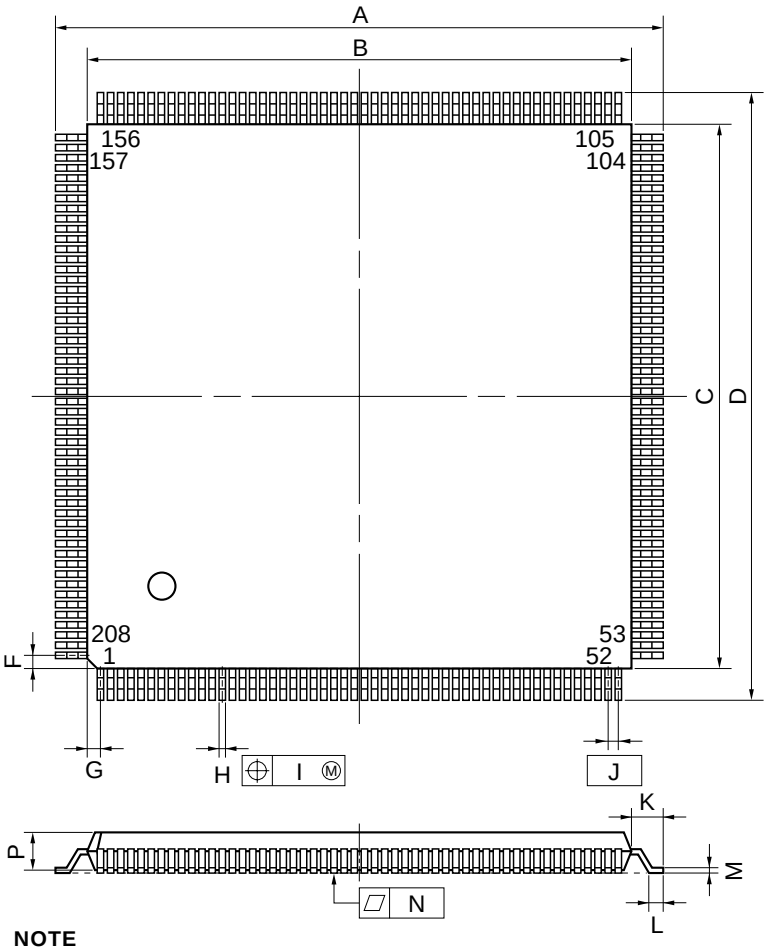
(3) 4 Mbytes



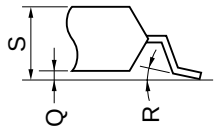
Recommended Devices 8-Mbit SGRAM : μPD481850GF-A12
16-Mbit SDRAM : μPD4516161G5-A10, μPD4516161G5-A12

PACKAGE DRAWING

208-PIN PLASTIC QFP (FINE PITCH) (28 × 28 mm)



detail of lead end



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	30.6±0.2	1.205±0.008
B	28.0±0.2	$1.102^{+0.009}_{-0.008}$
C	28.0±0.2	$1.102^{+0.009}_{-0.008}$
D	30.6±0.2	1.205±0.008
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.3±0.2	0.051±0.008
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	3.2	0.126
Q	0.4±0.1	$0.016^{+0.004}_{-0.005}$
R	5°±5°	5°±5°
S	3.8 MAX.	0.150 MAX.

P208GD-50-LML, MML-2

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[MEMO]

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M7A 96.10

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