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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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PowerVR™ PCX1™

Three-Dimensional Graphics PC Processor

μPD62010

DESCRIPTION

Developed jointly by NEC and VideoLogic, PowerVR is the future of high-quality, three-dimensional graphics for the next generation of interactive entertainment.

PowerVR architecture eliminates the need for Z-buffer memory, reducing system cost and removing the Z-buffer bandwidth bottleneck. By adding a single SGRAM/SDRAM for textures and local parameters, the PCX1 becomes a powerful, cost-effective, three-dimensional graphics accelerator for PC platforms.

PowerVR PCX1 is a single chip combining an Image Synthesis Processor™ (ISP) for shadow generation and depth cuing, a Texture and Shading Processor™ (TSP) for MIP-mapped, perspective-correct textures and high-quality shading, and a high-performance master/slave interface. Using DirectDraw™, rendered images are transferred over the PCI bus to the VGA controller's frame buffer for display. The PowerVR PCX1 is independent of the VGA controller, allowing it to be used with a wide range of PCs.

FEATURES

- 66-MHz operating speed
- 32 processing elements in the image synthesis module
- 32-bit depth precision
- On-chip hidden surface removal eliminates need for Z-buffer memory
- On-chip 12K ISP and 4K TSP parameter caches
- Single SGRAM/SDRAM external interface for texture and parameter caching
- Perspective-correct texturing
- PCI 2.1 interface
- True shadow generation and per pixel fogging
- Perspective-correct texturing
- 32 × 32 to 256 × 256 texture bitmap sizes
- 1- to 4-Mb SGRAM/SDRAM texture memory
- Multiple texture formats; anti-aliased
- 16- and 24-bit video formats including dithering
- Smooth shading
- Flat shading with offset highlights
- Exponential fogging; programmable fog color
- Multiple translucent textures and layers
- Global translucency allows objects to fade (16 levels)
- Software support
 - Microsoft® Direct3D™ driver support
 - PowerVR SGL graphics language three-dimensional graphics application programming interface (API), and library

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PCX1, Image Synthesis Processor, and Texture and Shading Processor are trademarks of NEC Corporation.

Microsoft is a registered trademark and Direct3D, DirectDraw, and Windows 95 are trademarks of Microsoft Corporation.

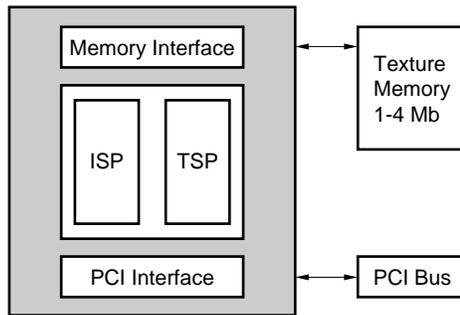
SOFTWARE SUPPORT

PowerVR is supported by several application programming interfaces (APIs).

These include Microsoft's Direct3D and the PowerVR SGL from NEC and VideoLogic. Direct3D support allows standard Windows 95™ titles to exploit PowerVR's capabilities. PowerVR SGL takes full advantage of PowerVR's features such as shadows and searchlights, and also provides a unified programming environment for console, PC, and arcade development.

PowerVR SGL is a high-level API that gives application developers access to PowerVR's advanced features. With this development system, the same code can be used to develop games for the arcade, PC platform, and console markets.

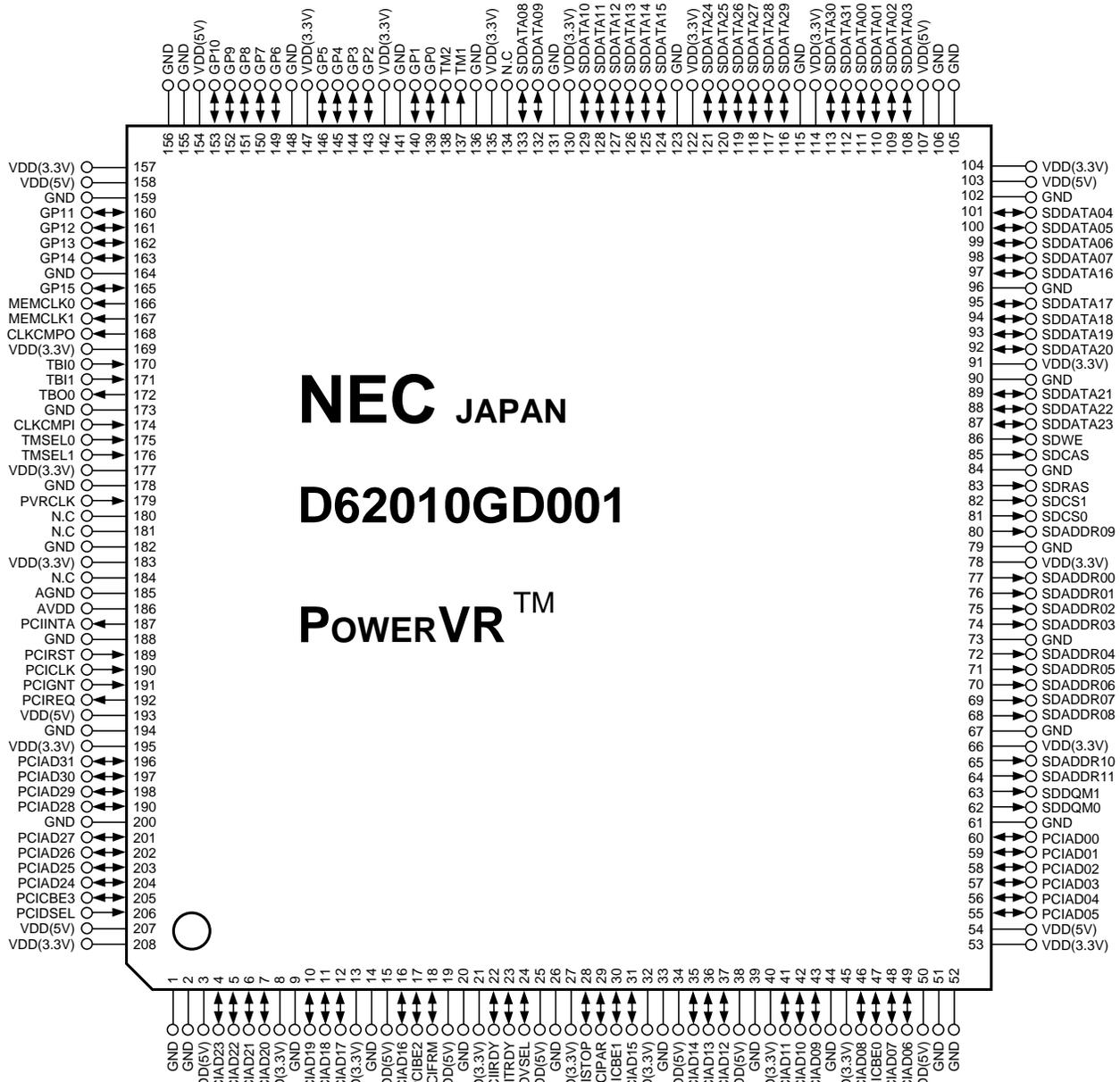
Three-Dimensional Graphics Accelerator PCI Card Solution



Phase-out/Discontinued

PIN CONFIGURATION (Top View)

208-pin plastic QFP (28 × 28)

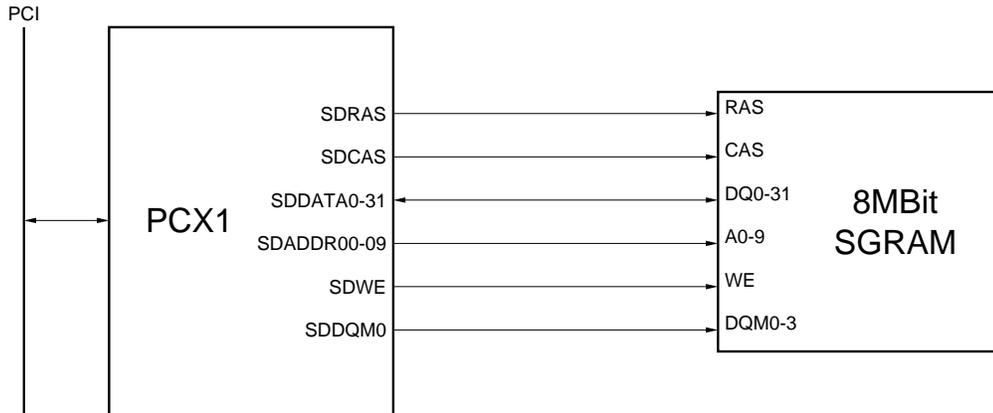


PIN FUNCTIONS

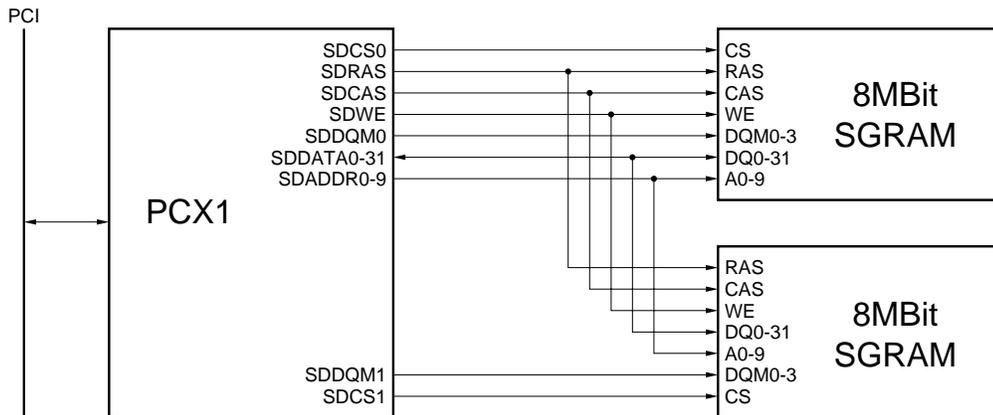
Name	Function
PCIFRM	PCI Cycle Frame
PCIIRDY	PCI Initiator Ready
PCITRDY	PCI Target Ready
PCIDVSEL	PCI Device Select
PCISTOP	PCI Stop/Disconnect
PCIPAR	PCI Parity
PCIINTA	PCI Interrupt A
PCIRST	PCI Reset, used as master reset for PCX1
PCICLK	Clock for PCI Interface
PCIGNT	PCI Master Grant
PCIREQ	PCI Master Request
PCICBE0-3	PCI Bus Command and Byte Enables
PCIIDSEL	PCI Initialization Device Select
PCIADD00-31	PCI Address Data Bus
SDDQM0-1	Memory Request
SDADR00-11	Memory Address Bus
SDCS0-1	Memory Chip Select
SDRAS	Memory Row Address Strobe
SDCAS	Memory Column Address Strobe
SDWE	Memory Write Enable
SDDATA00-31	Memory Data Bus
GP0-15	General Purpose I/O Port
MEMCLK0-1	Memory Clock
CLKCMPO	Clock Adjusting Port (Output)
CLKCMPI	Clock Adjusting Port (Input)
PVRCLK	Internal Clock
TM1-2	Test Input
TBI0-1	Test Input
TBO0	Test Output
TMSEL0-1	Test Input
VDD (5)	Digital VDD (5 V)
VDD (3.3)	Digital VDD (3.3 V)
GND	Digital GND
AVDD	Analog VDD
AGND	Analog GND

PCX1 MEMORY INTERFACE

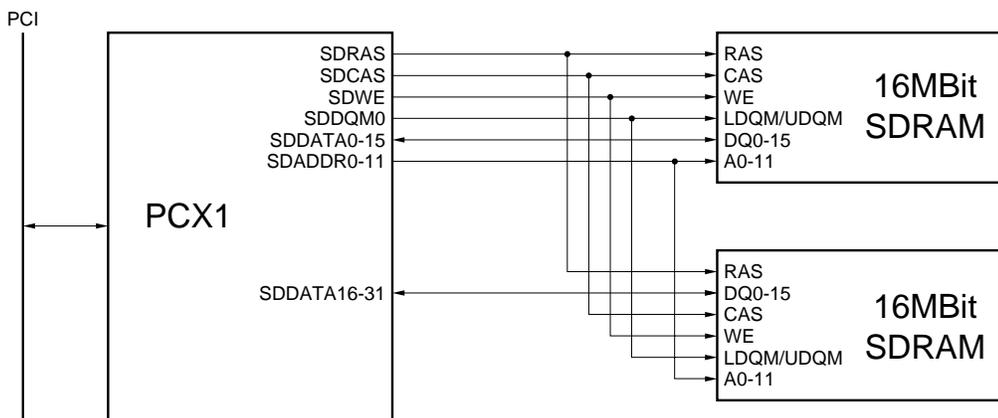
(1) 1 MByte



(2) 2 MByte



(3) 4 MByte



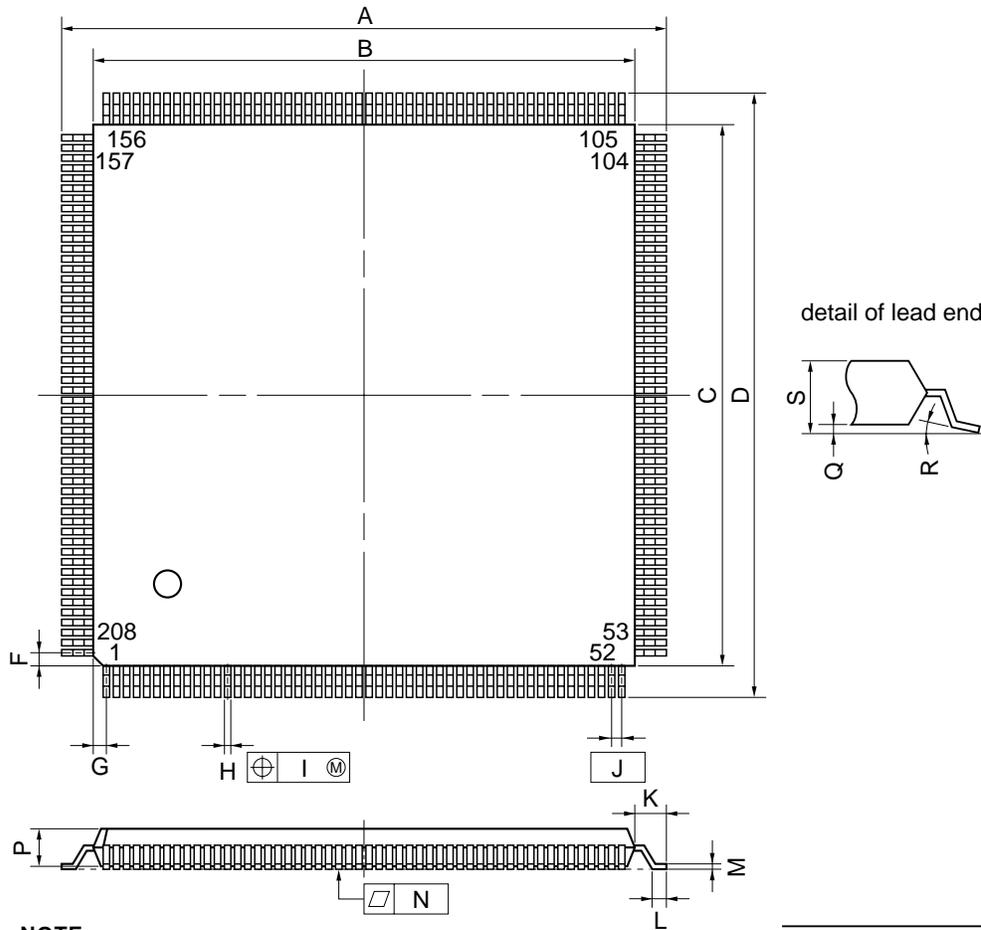
Recommended device

- 8 MBit SGRAM : μ PD481850GF-A12
- 16 MBit SDRAM: μ PD4516161G5-A10
- μ PD4516161G5-A12
- μ PD4516161G5-A67-PC

Phase-out/Discontinued

PACKAGE DRAWING

208 PIN PLASTIC QFP (FINE PITCH) (□ 28)



NOTE
Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	30.6±0.2	1.205±0.008
B	28.0±0.2	1.102 ^{+0.009} _{-0.008}
C	28.0±0.2	1.102 ^{+0.009} _{-0.008}
D	30.6±0.2	1.205±0.008
F	1.25	0.049
G	1.25	0.049
H	0.22 ^{+0.05} _{-0.04}	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.3±0.2	0.051±0.008
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.17 ^{+0.03} _{-0.07}	0.007 ^{+0.001} _{-0.003}
N	0.10	0.004
P	3.2	0.126
Q	0.4±0.1	0.016 ^{+0.004} _{-0.005}
R	5°±5°	5°±5°
S	3.8 MAX.	0.150 MAX.

P208GD-50-LML, MML-2

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