V6388B

(VPDC)

■ OUTLINE

The versatile panel display controller (VPDC) is a high-level display controller with functions for controlling large-capacity flat panel displays (hereinafter simply "panels") and for controlling raster-scanning CRT displays. In addition, since application software written for CRTs can be used as is when the VPDC BIOS is used, portable and transportable computers with panels can be configured easily. (Display switching between CRT and panel as necessary is possible.) This VPDC is completely compatible with the IBM-PS/2 video graphics array (VGA). When a standard monitor is used, this compatibility requires no change to the BIOS or software whatsoever. Even if a non-standard monitor is used, compatibility can be achieved by simply setting the values of switches with the VPDC BIOS. There is no need to change the software at all. For example when an IBM monochrome monitor and 2-tone panel are used, color display software can be executed. (Monitors that can not display colors handle this with gray scaling and hatching.)

It can also be easily configured for higher level display systems, with a built-in color look-up table (LUT) for color mapping.

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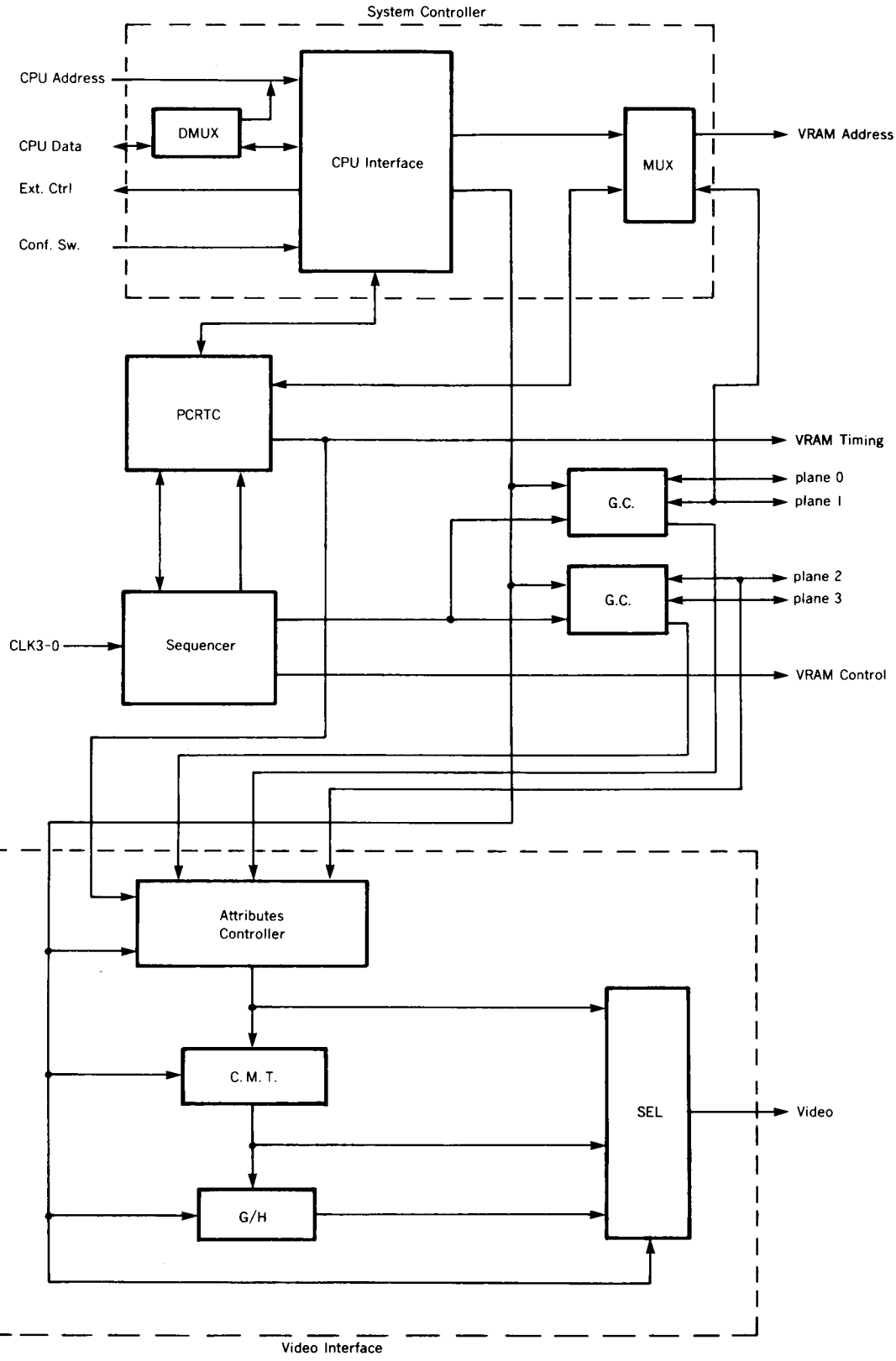
V6388B CATALOG
CATALOG No. :LSI-216388X
1990. 7

■ FEATURES

- Compatible with the IBM VGA and register level (when CRT is used); CPU interface is PC-BUS specification.
- Since all the functions of the VGA have been included, the VGA board functions can be realized with few parts for IBM PC compatibles. Furthermore, LCD, plasma displays, and EL displays can be controlled as well.
- The VPDC can be connected to the following CRTs:
  - · IBM monochrome display
  - · IBM color display
  - · IBM enhanced color display
  - · NEC Multisync monitor (and models from other manufacturers that have the same functions)
  - · IBM 8503 monochrome display
  - · IBM 8512 color display
  - · IBM 8513 color display
- The VPDC can be connected to panels (LCD, plasma, EL and various other panels) with the following resolutions:
  - · 640 x 200 · 320 x 200
  - · 640 x 400 · 720 x 400
  - · 640 x 480 · 640 x 350
- Eight 64K x 4 dynamic RAM chips or eight 32K x 8 static RAM chips can be used for video RAM (for a maximum of 256 KB)
- Up to 16 colors can be displayed for 640 x 480 dots.
- 1-screen panels and 2-screen panels can be used.
- The duty cycle can be set as high as 1/512 when a 2-screen panel is used.
- The AC signal for the LCD panel can be set freely in units of 1Horizontal scan (with a maximum pulse width of 1024H).
- Data can be sent to the panel in parallel 4 or 8 bits at a time or serially.
- Color liquid crystal displays can be used (up to 64 colors can be displayed).
- 16-shade display is possible with panels and monochrome monitors. (Of these 16, 9 can be converted into 9 hatching patterns.)
- Screen display position compensation is possible when using panels the same as for CRTs (Screen center can also be adjusted).
- Multi-raster scan function (display taking into account the aspect ratio)
- Built-in look-up table (LUT) for color mapping
- CMOS, 128-pin QFP

■ BLOCK DIAGRAM



■ PIN FUNCTIONS

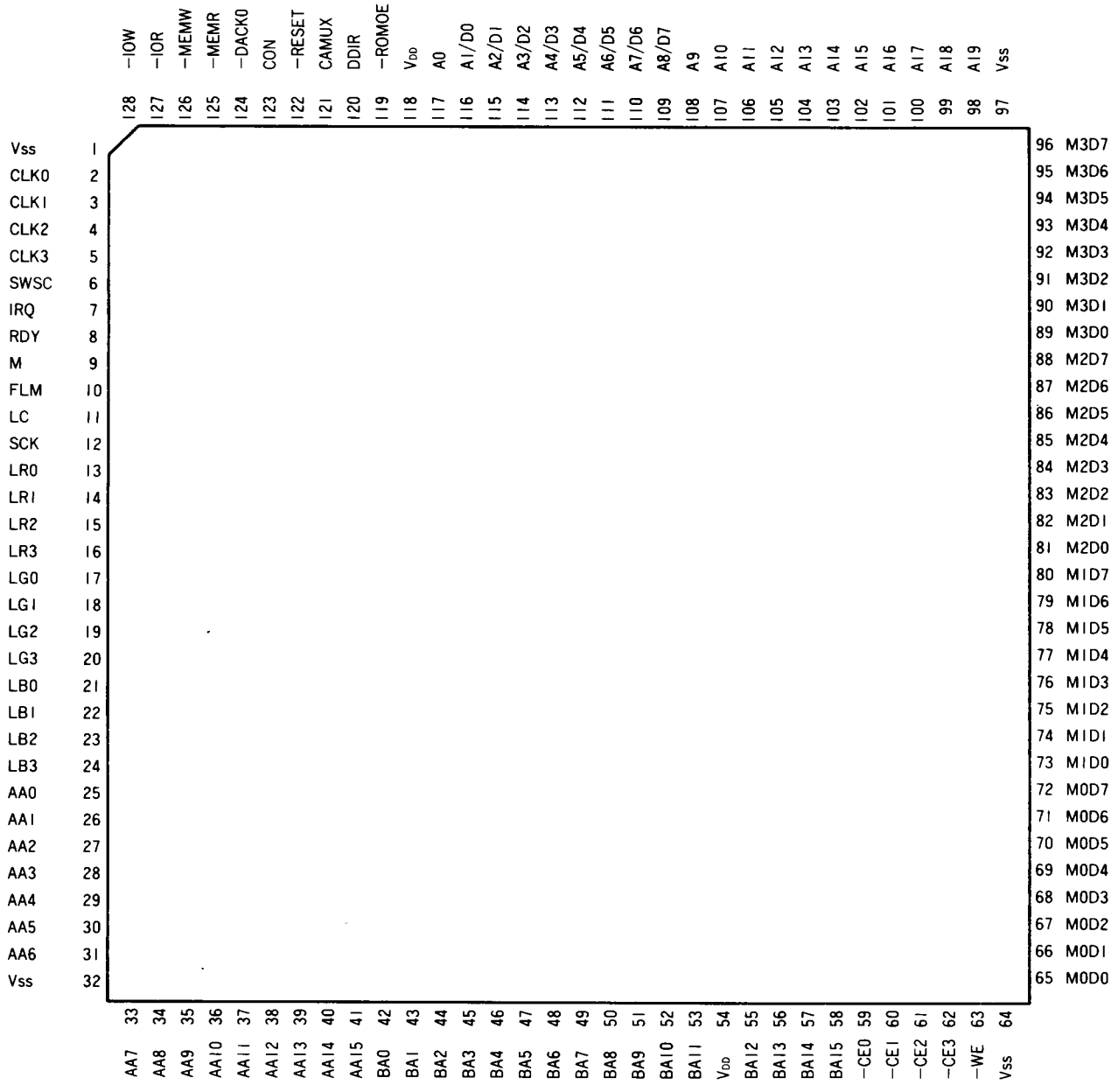
Signal	I/O	Number of pins	Pin function	
A19-9, 0	I	12	CPU Address Bit 19-9, 0	
A8/D7-A1/D0	I/O	8	CPU Address bit 8-1/CPU Data bit 7-0	
CAMUX	I	1	Address and data multiplex signal	
DDIR	O	1	Data bus direction control	
–ROMOE	O	1	BIOS ROM read out control	
–DACK0	I	1	CPU refresh timing	
–MEMR	I	1	Control for read out from memory	
–MEMW	I	1	Control for writing to memory	
–IOR	I	1	Control for read out from I/O registers	
–IOW	I	1	Control for writing to I/O registers	
RDY	O	1	Ready	
–RESET	I	1	Power On Reset	
IRQ	O	1	Interrupt Request	
CLK3-0	I	4	Clock input (25 MHz/28 MHz/Extclk/other)	
SWSC	I	1	Switch sense input	
CON	O	1	External control signal output	
VDD	I	2	+5V	
VSS	I	4	Ground	CPU
LR3-0	O	4	Panel display data (red)	
LG3-0	O	4	Panel display data (green/bottom screen)	
LB3-0	O	4	Panel display data (blue/top screen)	
SCK	O	1	Panel shift clock	
LC	O	1	Panel data latch clock	
FLM	O	1	Panel scan start signal	
M	O	1	Panel AC signal	pannel
LB3	O	1	–DACIOW: VIDEO DAC write control	
LB2	O	1	–DACIOR: VIDEO DAC readout control	
LB1,0	O	2	Non Connection	
LG 3-0	O	4	P7-4: PEL Address Inputs bit 7-4	
LR 3-0	O	4	P3-0: PEL Address Input bit 3-0	
LC	O	1	HSY: horizontal sync signal	
FLM	O	1	VSY: vertical sync signal	
SCK	O	1	DCLK: dot clock for VIDEO DAC	
M	O	1	–BLANK: blank for VIDEO DAC	CRT (VGA)

Signal	I/O	Number of pins	Pin function	
LB 3-0	O	4	Non Connection	
LG 3,2	O	2	Non Connection	
LG 1	O	1	R': Secondary Red	
LG 0	O	1	G'/I: Secondary Green/Intensity	
LR 3	O	1	B'/M: Secondary Blue/Monochrome	
LR 2	O	1	R: Primary Red	
LR 1	O	1	G: Primary Green	
LR 0	O	1	B: Primary Blue	
LC	O	1	HSY: horizontal sync signal	
FLM	O	1	VSY: vertical sync signal	
SCK	O	1	DCLK: Dot Clock	
M	O	1	—BLANK: Blank Timing	CRT (EGA)
AA15-0	O	16	VRAM Address for Plane 0 and 1	
BA15-0	O	16	VRAM Address for Plane 2 and 3	
—CE3-0	O	4	VRAM Chip Enable for Plane 3-0	
—WE	O	1	VRAM Write Enable	
M0D7-0	I/O	8	VRAM Data for Plane 0	
M1D7-0	I/O	8	VRAM Data for Plane 1	
M2D7-0	I/O	8	VRAM Data for Plane 2	
M3D7-0	I/O	8	VRAM Data for Plane 3	SRAM
AA7-0	O	8	VRAM Address for Plane 0 and 1	
BA7-0	O	8	VRAM Address for Plane 2 and 3	
BA15,14	I	2	FCIN 1,0: Feature Code 1,0	
BA13,12	O	2	FCOUT 1,0: Feature Control 1,0	
AA11	O	1	—CAS: Column Address Strobe	
—CE3-0	O	4	—RAS3-0: Row Address Strobe for Plane 3-0	DRAM

For power on reset Signal

Signal	I/O	Number of pins	Pin function
BA15-8	I	8	Configuration switches input

■ PIN LAYOUT



■ ELECTRICAL CHARACTERISTICS

Absolute maximum ratings (with Vss = 0.0V as the standard)

Item	Symbol	Min.	Max.	Unit
Power supply voltage	V_{DD}	−0.3	7.0	V
Input voltage	V_I	−0.3	V_{DD}+0.3	V
Output voltage	V_O	−0.2	V_{DD}+0.3	V
Operating ambient temperature	T_{OP}	0	70	°C
Storage temperature	T_{STG}	−50	125	°C

Recommended operating conditions (with Vss = 0.0V as the standard)

Item	Symbol	Min.	Typical	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating ambient temperature	T_{OP}	0	25	70	°C
Low level input voltage*	V_{IL}			0.8	V
High level input voltage*	V_{IH}	2.2			V

*: except for clock input

Pin capacitance

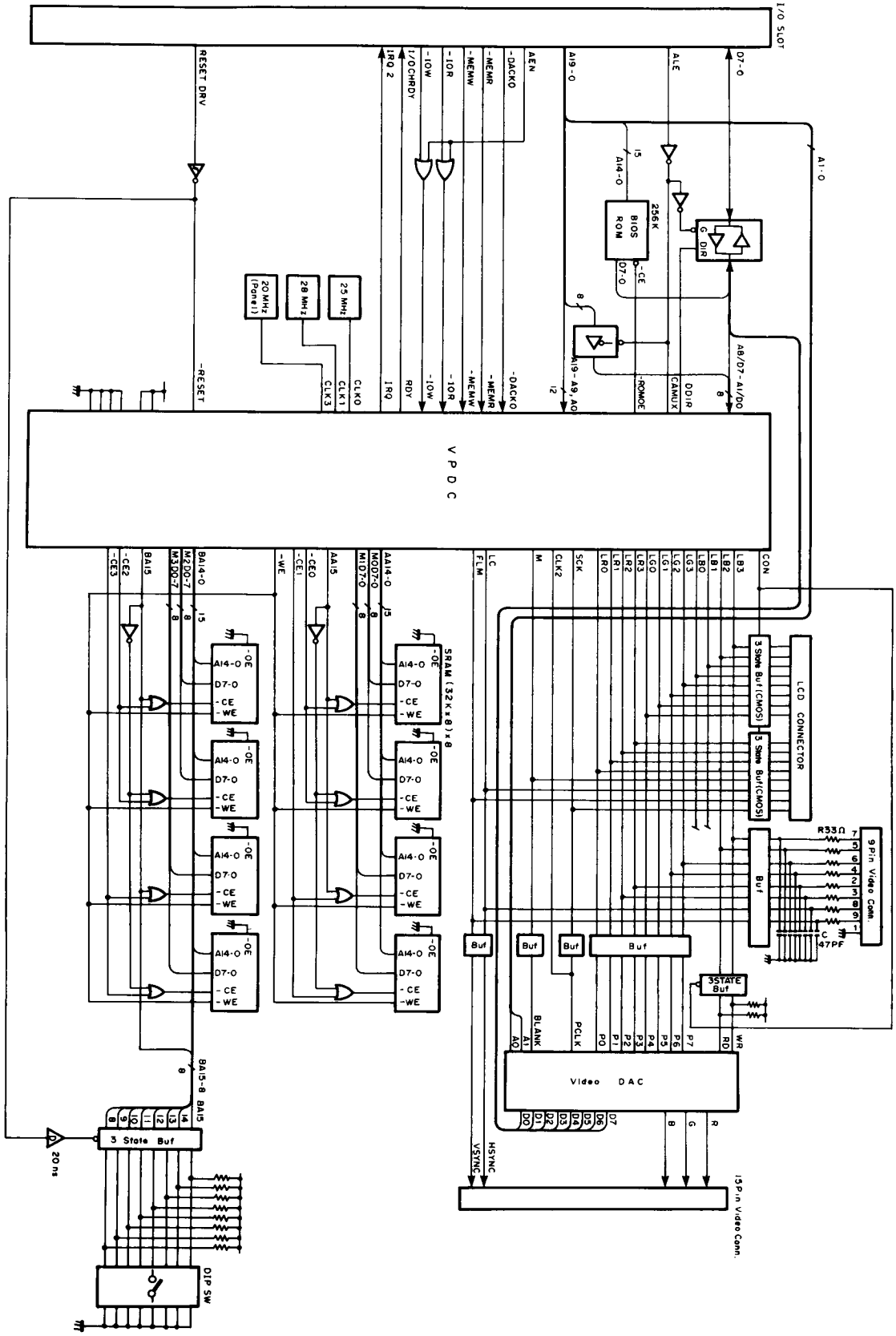
Measurement conditions: Top = 25.0°C V_{DD} = 5.00V
V_{IH} = 2.4Vmin. V_{IH} = 0.8Vmax.
Input signal frequency: 1.0MHz
Except V_{DD} and the pin being measured, perform measurement with connections made to GND.

Item	Symbol	Min.	Typical	Max.	Unit
Input pin capacitance	C_I			8	pF
Output pin capacitance	C_O			10	pF
Input/output pin capacitance	C_{IO}			12	pF

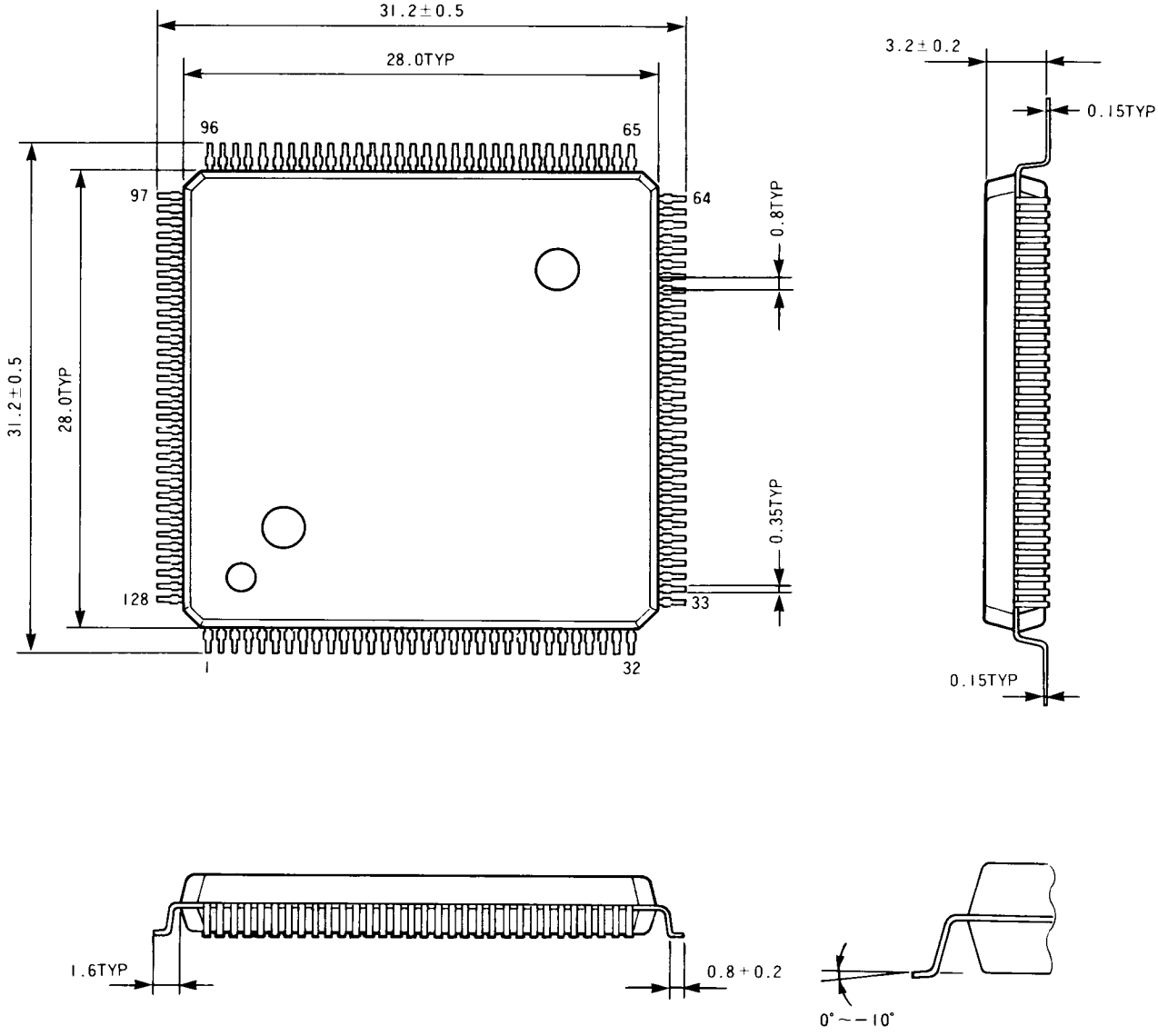
DC characteristics (at recommended operating conditions)

Item	Symbol	Condition	Min.	Max.	Unit
High level output voltage	V_{OH}	I_{OH} = −80μA	2.4		V
Low level output voltage	V_{OL}	I_{OL} = 1.6mA		0.4	V
Input leak current	I_L		−10	10	μA
Power supply current	I_{DD}			175	mA

■ EXAMPLE OF SYSTEM CONFIGURATION (SRAM AND CRT)



■ EXTERNAL DIAGRAM OF THE PACKAGE



The specifications of this product are subject to improvement changes without prior notice.

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